



Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

What is claimed is:

1. (original) A multilayer printed circuit board (PCB) interface comprising:  
a top PCB layer, a top surface of said top PCB layer for receiving at least one top module;  
a middle PCB layer including an electrically conductive layer disposed between two dielectric layers, said electrically conductive layer forming a plurality of connectors protruding horizontally for coupling the PCB interface to a main board; and  
a bottom PCB layer, a bottom surface of said bottom PCB layer for receiving at least one bottom module.
2. (original) The multilayer PCB of claim 1 wherein said top PCB layer further includes a top electrically conductive layer, a dielectric core, and a bottom electrically conductive layer.
3. (original) The multilayer PCB of claim 2 wherein said top electrically conductive layer includes a plurality of traces forming a predetermined circuit pattern.
4. (original) The multilayer PCB of claim 1 wherein said bottom PCB layer includes a top electrically conductive layer, a dielectric core, and a bottom electrically conductive layer.
5. (original) The multilayer PCB of claim 4 wherein said bottom electrically conductive layer includes a plurality of traces forming a predetermined circuit pattern.

6. (original) The multilayer PCB of claim 1 wherein said top surface of said top PCB layer is configured to receive a plurality of packaging technologies.
7. (original) The multilayer PCB of claim 1 wherein said bottom surface of said bottom PCB layer is configured to receive a plurality of packaging technologies.
8. (original) The multilayer PCB of claim 1 wherein said electrically conductive layer includes copper having a density of about 5 ounces per square inch.
9. (original) The multilayer PCB of claim 1 wherein said plurality of connectors forms a TSOP connection with a surface of said main board.
10. (original) A multichip IC packaging comprising:
  - a multilayer PCB having a top surface, a bottom surface, and a middle electrically conductive layer forming a plurality of connectors protruding horizontally from said multilayer PCB, said plurality of connectors for coupling to a main board;
  - a first plurality of modules coupled on said top surface; and
  - a second plurality of modules coupled on said bottom surface.
11. (withdrawn) A method for connecting a multilayer PCB to a main board comprising:
  - mounting a plurality of modules on a top surface of a top PCB layer and a bottom surface of a bottom PCB layer of the multilayer PCB, said multilayer PCB including a middle electrically

conductive layer protruding from said multilayer PCB and forming a plurality of connectors; and  
coupling said plurality of connectors to a surface of the main board.

12. (withdrawn) The method of claim 11 wherein said top PCB layer includes a top electrically conductive layer, a dielectric core, and a bottom electrically conductive layer.

13. (withdrawn) The method of claim 12 wherein said top electrically conductive layer includes a plurality of traces forming a predetermined circuit pattern.

14. (withdrawn) The method of claim 11 wherein said bottom PCB layer includes a top electrically conductive layer, a dielectric core, and a bottom electrically conductive layer.

15. (withdrawn) The method of claim 14 wherein said bottom electrically conductive layer includes a plurality of traces forming a predetermined circuit pattern.

16. (withdrawn) The method of claim 11 wherein said top surface of said top PCB layer is configured to receive a plurality of packaging technologies.

17. (withdrawn) The method of claim 11 wherein said bottom surface of said bottom PCB layer is configured to receive a plurality of packaging technologies.

18. (withdrawn) The method of claim 11 wherein said electrically conductive layer includes copper having a density of about 5 ounces per square inch.

19. (withdrawn) The method of claim 11 wherein said plurality of connectors forms a TSOP connection with said surface of the main board.
20. (original) A multilayer printed circuit board (PCB) interface comprising:
- means for receiving at least one top module;
  - means for receiving at least one bottom module; and
  - means for coupling the PCB interface to a main board.
21. (original) The multilayer PCB of claim 20 wherein said at least one top module includes a plurality of packaging technologies.
22. (original) The multilayer PCB of claim 20 wherein said at least one bottom module includes a plurality of packaging technologies.
23. (original) The multilayer PCB of claim 20 wherein said means for coupling includes a TSOP connection with said main board.